

PRELIMINARY
 Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS M37790SJ, M37790STJ

■ 6249828 0013642 6 ■

16-BIT CMOS MICROCOMPUTER

MITSUBISHI (MICMPTR/MIPRC) 29E D T.49-19-59

DESCRIPTION

The M37790SJ, and the M37790STJ are 16-bit microcomputers designed with high-performance CMOS silicon gate technology. These are housed in a 84-pin PLCC. These microcomputers have a large 16M bytes address space, the instruction queue buffers, and the data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. Utilizing its built-in peripheral functions such as timer system, 10-bit A-D converter and pulse width modulator (PWM), the M37790SJ and the M37790STJ are especially suited for industrial machinery applications that require real time control capability. The M37790STJ is a version of the M37790SJ that has been upgraded for use in automobile vehicles. Its function and performance are same as for the M37790SJ, but it has a different operating temperature range which is shown below:

Type name	Operating temperature range
M37790SJ	-20~75°C
M37790STJ	-40~80°C

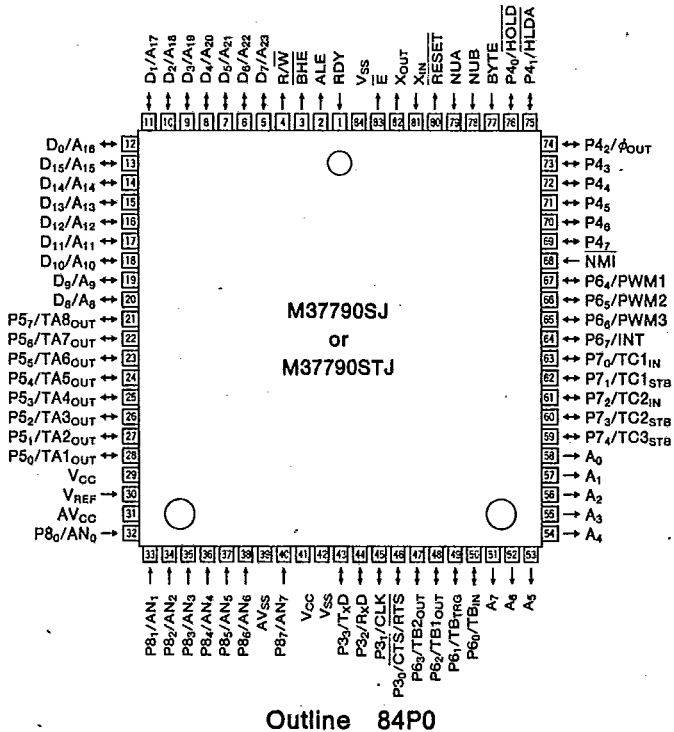
DISTINCTIVE FEATURES

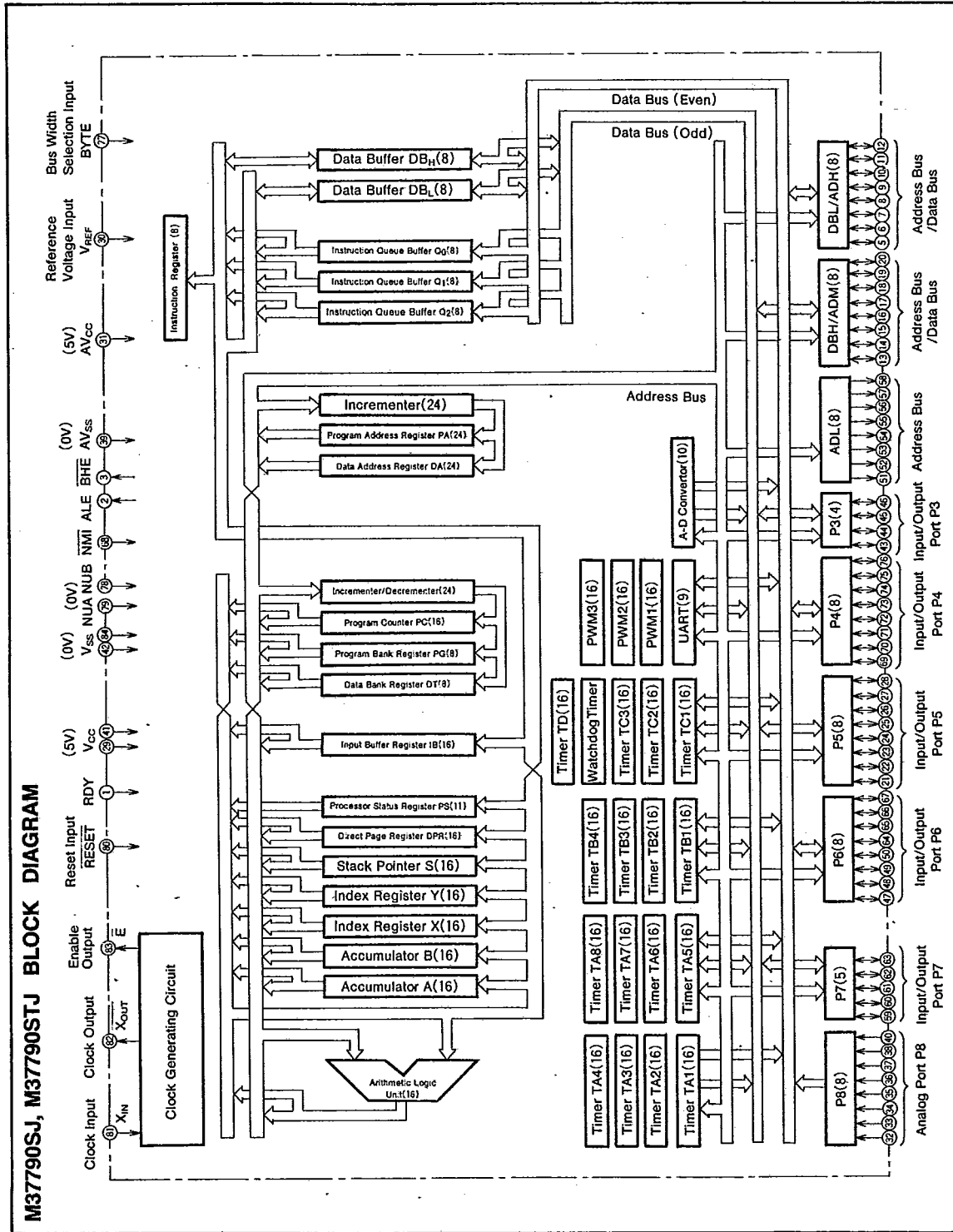
- Number of basic instructions.....103
- Instruction execution time
 (The fastest instruction at 8 MHz frequency)500 ns
- Single power supply.....5V±10%
- Low power dissipation (at 8 MHz frequency).....100mW
- Memory.....ROM/RAM external
- Interrupt.....20 types, 7 level
- 16-bit timer.....16
- PWM.....3
- UART (may also be synchronous).....1
- 10-bit A-D converter.....8 channel input
- Watchdog timer.....1
- Programmable input/output
 (ports P3, P4, P5, P6, P7,).....33

APPLICATION

For factory automation system, automobiles and other industrial machinery control.

PIN CONFIGURATION (TOP VIEW)





16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37790SJ, M37790STJ

Parameter		Functions
Number of Basic Instructions		103
Instruction Execution Time		500ns
Memory		ROM/RAM external
Input/Output Port	P4~P6	8-bitX3
	P3	4-bitX1
	P7	5-bitX1
Analog Input Port	P8	8-bitX1
16-bit Timer	Real-time Output Timer	16-bitX8
	Cascade timer	16-bitX4
	Input Signal Measurement Timer	16-bitX3
	Free-run timer	16-bitX1
PWM		8-bitX3
A-D converter		10-bitX1 (8 channels)
Serial I/O		(UART or Clock Synchronous)X1
Watchdog Timer		12-bitX1
Interrupts		20 types: Maskable Interrupt factor is capable of setting the Interrupt Priority Level (IPL) of 0 to 7 for each factor.
Clock Generating Circuit		Built-in (externally connected ceramic or quartz crystal oscillator)
Supply Voltage		5V±10%
Power Dissipation		100mW
Operating Temperature Range	M37790SJ	-20~75°C
	M37790STJ	-40~85°C
Device Structure		CMOS high-performance silicon gate process
Package		84-pin PLCC

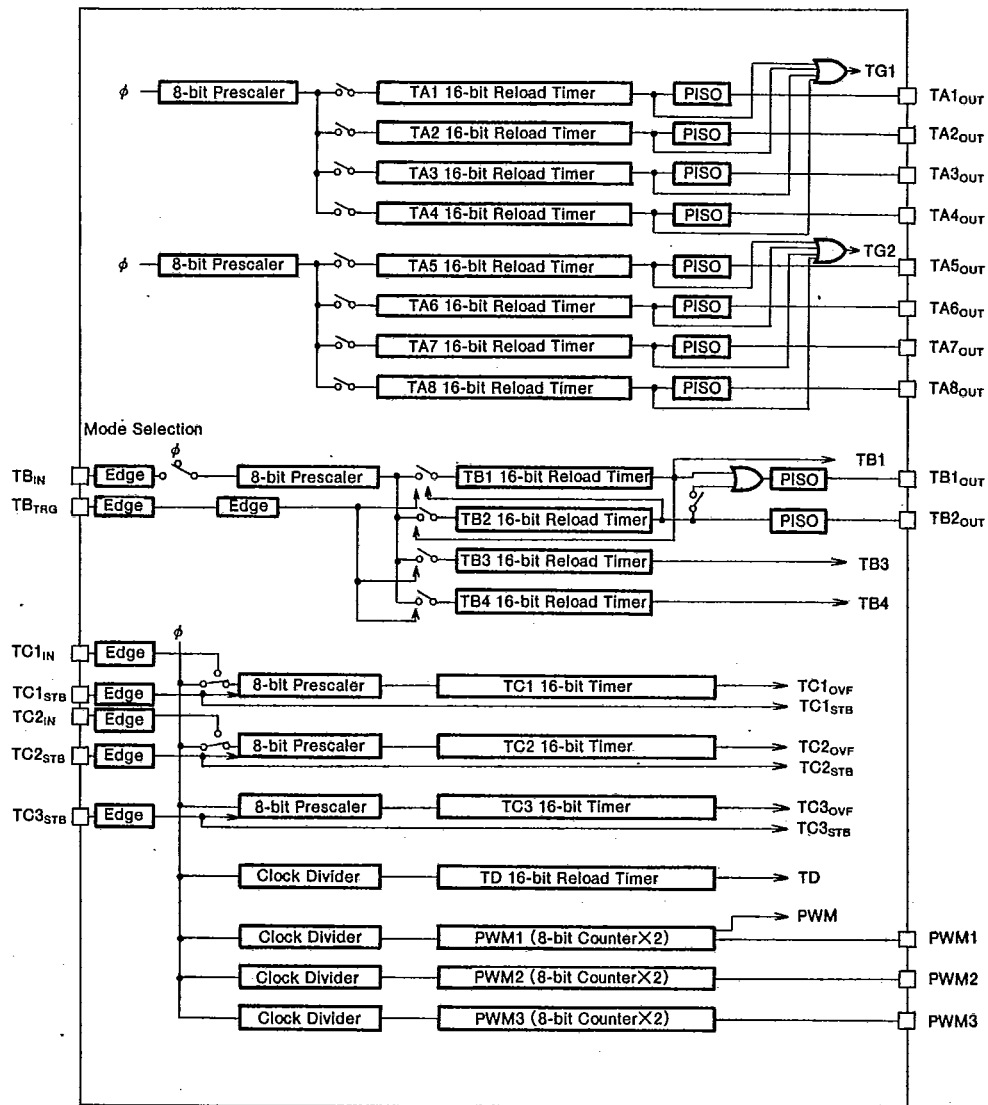
PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Power supply		Supply 5V±10% to V _{CC} and 0V to V _{SS} .
RESET	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X _{IN} and X _{OUT} . When an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
NUA, NUB	Not usable	Input	These pins are connected to GND.
RDY	Ready signal input	Input	When this pin's level is "L", the internal clock ϕ stays at the "L" level.
\bar{E}	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	This pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8-bit when "H" signal inputs.
NMI	Non-maskable interrupt input pin	Input	This is the non-maskable interrupt input pin. This interrupt used to control the debugger, etc. Users are not allowed to use this.
\bar{BHE}	Byte high enable output	Output	"L" level is output when an odd-numbered address is accessed.
ALE	Address latch enable output	Output	This signal is used to retrieve only the address data from address data and data multiplex signal.
R/ \bar{W}	Read/Write signal output	Output	This signal indicates the data bus status, "H" indicates the read status and "L" indicates the write status.
AV _{CC} , AV _{SS}	A-D power supply	Input	Power supply for the A-D converter.
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
A ₀ ~A ₇	Address bus (low-order)	Output	Low-order 8 bits address bus is output.
D ₈ /A ₈ ~D ₁₅ /A ₁₅	Data bus (high-order)/ Address bus (middle-order)	I/O	Multiplex signal consisting of middle-order 8 bits of address bus and high-order 8 bits of data bus is input/output.
D ₀ /A ₁₆ ~D ₇ /A ₂₃	Data bus (low-order)/ Address bus (high-order)	I/O	Multiplex signal consisting of high-order 8 bits of address bus and low-order 8 bits of data bus is input/output.
P ₃₀ ~P ₃₃	I/O port P3	I/O	This is a CMOS input/output port. All 4 bits have double functions, which can be selected by software.
$\overline{CTS/RTS}$	Transmit enable signal	I/O	This pin controls serial I/O transmitting.
CLK	Transmit/Receive clock	I/O	This is the serial I/O clock input/output.
RxD	Receive data	Input	This is the input pin for serial I/O.
TxD	Transmit data	Output	This is the output pin for serial I/O.

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Pin	Name	Input/Output	Functions
P4 ₀ ~P4 ₇	I/O port P4	I/O	This is a CMOS input/output port. P4 ₀ , P4 ₁ and P4 ₂ have double functions, which can be selected by software.
$\overline{\text{HOLD}}$	Hold request signal	Input	This is the hold request input to the CPU. Input of "L" level sets the CPU in the hold status when the currently executing bus cycle is finished. Input of "H" level releases the hold and the CPU resumes execution.
$\overline{\text{HLDA}}$	Hold acknowledge signal	Output	When CPU is in the hold status, "L" level signal is output.
ϕ_{OUT}	System clock output	Output	This is the external output of CPU system clock (ϕ).
P5 ₀ ~P5 ₇	I/O port P5	I/O	This is a CMOS input/output port. All 8 bits have double functions, which can be selected by software.
TA1 _{OUT} ~TA8 _{OUT}	Timer driven output	Output	These output signals update by synchronizing with the timer underflow, etc. of the timers, TA1~TA8.
P6 ₀ ~P6 ₇	I/O port P6	I/O	This is a CMOS input/output port. All 8 bits have double functions, which can be selected by software.
TB _{IN}	Timer B clock	Input	This signal is used as the clock input for the timers, TB1~TB4.
TB _{TRG}	Timer B trigger	Input	This is the trigger signal input for the one-shot function of the timers, TB1, TB3 and TB4.
TB1 _{OUT}	Timer driven output	Output	These output signals update data by synchronizing with the timer underflow, etc. of the timers, TB1 and TB2.
PWM1~PWM3	PWM output	Output	Output pulse of this pin is generated by PWM.
INT	External interrupt input	Input	This is the interrupt input pin. Edge sense or level sense can be specified.
P7 ₀ ~P7 ₄	I/O port P7	I/O	This is a CMOS input/output port. All 5 bits have double functions, which can be selected by software.
TC1 _{IN}	Timer C1 clock	Input	This is the timer TC1's clock input.
TC1 _{STB}	Timer C1 strobe	Input	This is the strobe signal input for timer TC1's measurement function.
TC2 _{IN}	Timer C2 clock	Input	This is the timer TC2's clock input.
TC2 _{STB}	Timer C2 strobe	Input	This is the strobe signal input for timer TC2's measurement function.
TC3 _{STB}	Timer C3 strobe	Input	This is the strobe signal input for timer TC3's measurement function.
P8 ₀ ~P8 ₇	Analog input port	Input	This is an 8-bit analog input pin to the A-D converter.

M37790SJ, M37790STJ TIMER SYSTEM BLOCK DIAGRAM

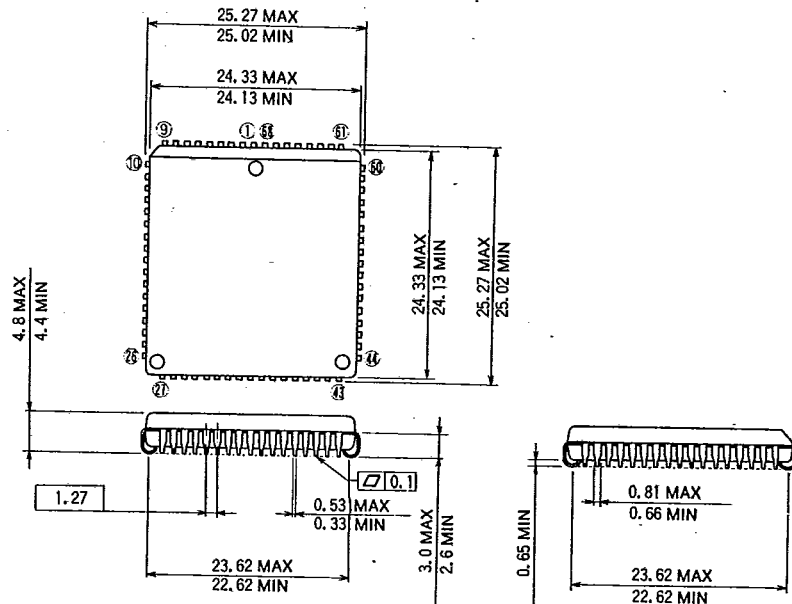


PACKAGE OUTLINES

T.90-20

TYPE 68P0 68-PIN MOLDED PLASTIC LEADED CHIP CARRIER

Dimension in mm



TYPE 80P6 80-PIN MOLDED PLASTIC QFP

Dimension in mm

